What is claimed is:

1. A method for forming an electrode, comprising:
forming a polysilicon layer on a semiconductor substrate;
forming an amorphous silicon capping layer on the polysilicon layer; and
depositing a silicide layer on the capping layer.

2. The method of claim 1, wherein the silicide layer is formed using a dichlorosilane (SiH_2Cl_2) gas, and wherein the capping layer is formed to have a thickness sufficient to prevent chlorine ions dissociated from the dichlorosilane (SiH_2Cl_2) gas from diffusing toward the polysilicon layer.

3. The method of claim 1, wherein a thickness of the amorphous silicon capping layer is not less than about 50Å.

4. The method of claim 1, wherein the polysilicon layer is formed by depositing polysilicon or by crystallizing amorphous silicon.

5. A method for forming a control gate electrode layer of a semiconductor device electrode in which a gate insulation layer, a polysilicon layer for a floating gate electrode, and an intergate dielectric layer are sequentially stacked on a semiconductor substrate, the method comprising:
a) forming an amorphous silicon layer on the intergate dielectric layer;
b) annealing the amorphous silicon to form a polysilicon layer;
c) forming an amorphous silicon capping layer on the polysilicon layer; and
d) forming a silicide layer on the capping layer, using dichlorosilane.

6. The method of claim 5, wherein the thickness of the amorphous silicon capping layer is not less than 50 Å.

7. The method of claim 5, wherein the silicide layer comprises tungsten silicide.

8. The method of claim 7, wherein forming the tungsten silicide layer comprises:

supplying a first silane (SiH_4) gas to a process chamber in which a wafer including the thin film of amorphous silicon is loaded;

supplying a dichlorosilane (SiH_2Cl_2) gas and a tungsten hexafluoride (WF_6) gas to the process chamber to deposit the tungsten silicide layer on the capping layer;

purging the dichlorosilane (SiH_2Cl_2) gas and the tungsten hexafluoride (WF_6) gas from the process chamber; and

supplying a second silane (SiH_4) gas to the process chamber.

9. The method of claim 5, wherein the annealing is performed in a nitrogen ambient.

10. A semiconductor memory device, comprising:

a gate oxide layer formed on a semiconductor substrate;

a floating gate electrode formed on the gate oxide layer;

an intergate dielectric layer formed on the floating gate electrode;

a polysilicon layer formed on the intergate dielectric layer;

a capping layer formed on the polysilicon layer; and

a silicide layer formed on the capping layer .

11. The device of claim 10, wherein the thickness of the capping layer is not less than 50Å.

12. The device of claim 10, wherein the capping layer comprises amorphous silicon.

13. The device of claim 10, wherein the polysilicon layer is formed by crystallizing amorphous silicon.

14. The device of claim 10, wherein the silicide layer comprises tungsten silicide.

15. The device of claim 14, wherein the tungsten silicide layer is formed using dichlorosilane.

16. The device of claim 10, wherein the capping layer is formed to a thickness sufficient to prevent chlorine ions from diffusing into the polysilicon layer, thereby preventing an abnormal growth of the polysilicon layer